A High-Precision Amplitude-Time to Digital Converter based on FPGA for Digital Multichannel Analyzer

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The article presents a high-precision Amplitude-Time to Digital Converter (A-TDC) for using in a Multichannel Analyzer (MCA). Utilizing this method, the MCA quantifies and statistically analyzes the discharge time of nuclear pulse signals, ultimately obtaining the gamma energy spectrum. The autonomous linear discharge circuit presented in this paper significantly simplifies the components and control logic of conventional discharge circuits. By leveraging the underlying logic of the FPGA's internal carry-chain, a delay chain capable of precise time measurement for both leading and trailing edges has been designed, which results in a substantial reduction in logical resource consumption. The high-resolution TDC designed based on the Xilinx Artix-7 series FPGA has a resolution of 69.4ps, and the average value of time measurement precision is 52.3ps. The linear discharge circuit has an inherent nonlinearity of less than 0.05%, and the overall linearity is better than 0.1%.When used in conjunction with a Φ 25mm×25mm NaI(Tl) detector for measuring the 662 keV full-energy peak of a ^{137}Cs source, the energy resolution achieved is 8.5%.

Keywords: Amplitude-time conversion; FPGA-TDC, Gamma energy spectrum, Constant current source discharges

1 Introduction

Digital multichannel analyzer has been extensively used in fields such as nuclear spectroscopy, environmental monitoring, nuclear accident response, and mineral resource exploration[1–7]. Digital pulse amplitude analyzers directly employ high-speed ADC for full waveform sampling of the pulse signal, followed by the devices such as Field Programmable Gate Array (FPGA) and Digital Signal Processing (DSP) to perform digital filtering, pulse shaping, and amplitude extraction on the digital signal[8, 9]. In applications requiring amplitude measurements of dozens, hundreds, or even thousands of channels, such as multichannel energy spectrum measurement, gamma irradiation imaging, and astronomical telescopes[10–14],the approach of using high-speed ADC for full measurements across each channel facing challenges in terms of system complexity, cost, and data communication.

Time-to-Digital Converter (TDC) has been used in various fields such as high-energy particle measurement and phase-locked loops since the 1980s [15–18]. TDC have transitioned from analog to digital[19], and researchers have studied vernier, passive interpolation, and gated ring oscillator TDC structures to improve timing resolution and measurement range. Some of these structures can achieve time resolution at the sub-gate level, and in certain applications, they can reach femtosecond (fs) level timing resolution [20–24].

TDC are primarily implemented using Application-Specific Integrated Circuit (ASIC) and FPGA. TDC systems based on ASIC offer better channel stability and consistency, whereas ASIC devices are complex to design, with high development costs. In contrast, FPGA-based TDC boast a short design cycle, high flexibility, low cost, and high temporal resolution. Some designs can achieve picoseconds-level resolution[25–29].

The amptitude of the pulse signal output from the detector is proportional to the energy deposited by the radiation or particles in it. By using a pulse peak detection and hold circuit, the pulse peak is stored in a holding capacitor. Then, a constant current source discharges the holding capacitor at a uniform rate, and the discharge time is proportional to the pulse amptitude. By measuring the discharging time, the energy deposited by the radiation can be accurately obtained.

Considering the strong competitiveness of FPGA-based high-precision TDC pulse amplitude analyzers in fields such as high-energy physics, radiation imaging, multichannel energy spectrum measurement, and gamma irradiation imaging [30, 31], this paper proposes an Amplitude-Time to Digital Converter for pulse amplitude measurement.

2 System Design

The high-precision A-TDC based on FPGA primarily consists of signal conditioning circuit and TDC in FPGA. Signal conditioning circuit mainly involves signal gain adjustment, peak-holding, constant-current discharge, and pulse-width conversion. The TDC in FPGA is comprised of an encoder (fine counter), a coarse counter, and a Processing Unit. The nuclear pulse signal output from the NaI(Tl) detector, after appropriate gain adjustment, is sent into a peak-holding and constant current discharge unit. This unit converts the nuclear pulse signals into single slope pulse signals whose widths are proportional to the peak of the nuclear pulse signals. Subsequently, a comparator transforms the single slope pulse signals into square wave signals., The widths of the square wave signals

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are proportional to the amplitudes of the original nuclear pulse signals and are measured by the TDC comprised by A fine counter based on the Delay chain and a coarse counter in the FPGA .

2.1 Automatic Peak-Holding and Constant Current Discharge

In low-channel measurement systems, specialized control signals can be designed to control the start and end of pulse discharging. However, in multi-channel measurement systems, configuring a discharging control circuit for each channel would significantly elevate circuit complexity and complicate the control logic. To accommodate multi-channel measurement systems, simplify control logic, and reduce circuit complexity, this paper employs an automatic peak-holding and constant-current source discharging method, as depicted in Fig. 1a.

After the gain adjustment, the input nuclear pulse signal proceeds into the automatic peak-holding circuit and the constant-current discharging circuit. Due to the direct-current bias power supply V_b and diodes D_1 and D_2, the incoming nuclear pulse signal charges the peak-holding capacitorC_h. The charge stored in the peak-holding capacitor is proportional to the signal peak value, $Q(t) = C \cdot V(1 - e^{-\frac{t}{\tau}})$.The constant-current discharging mechanism is realized through the cooperation of transistor Q_1 and resistors R_{dis}, R_1, and R_2.According to the voltage characteristics of the NPN(Negative-Positive-Negative) transistor base-emitter, V_b provides a stable static operating point for the Q_1 base after the voltage drop of the two diodes, so that the triode can work stably in the amplifier area during the discharge process, and the V_{be} is a constant value of about 0.6V. During the discharging process, V_{be} maintains a constant value of approximately 0.6V and the current fluctuation into the base of Q_1 is less than 0.05μA, so its influence can be disregarded. By connecting resistor R_{dis} in parallel between the base and emitter of Q_1, the discharge current of C_h is directed through R_{dis}. Additionally, since V_{be} remains constant, the current flowing through resistor R_{dis} during discharging remains consistent at $I \approx \frac{V_{be}}{R_{dis}}$, facilitating the achievement of constant-current discharging.

Upon the arrival of the nuclear pulse signal, the capacitor C_h undergoes swift charging. Due to the exceptionally brief rise time of the nuclear pulse signal, the voltage across C_h rapidly attains the peak value of the signal. The presence of V_b positions transistor Q_1 within its amplification zone. Simultaneously, as the input nuclear pulse signal charges C_h, the constant-current discharging circuit operates to concurrently discharge it. Consequently, a minor charge loss occurs during the charging phase, leading to a divergence between the peak voltage achieved by capacitor C_h and the peak value V_{amp} of the nuclear pulse signal. This discrepancy is influenced by both the rise time of the nuclear pulse signal and the magnitude of the discharging current.

Using the NaI(Tl) detector as an illustrative example, the input signal's rise time ranges between 100 nanoseconds (ns) and 300 ns. With a constant discharge current of 6 microamperes (μA),) and an input signal amplitude of 1 volt (V), the peak voltage experiences a reduction of 60 millivolts (mV). It is evident that the constant current discharge influences the capacitor's peak voltage by approximately 6%, while having a negligible impact on the amplitude conversion process.To maintain a uniform discharge process, a diode D_2 is placed above C_h. During the slow discharge of C_h, D_2 remains in the cutoff state, allowing current to flow only towards the subsequent circuit, the discharge current I_{dis} determining the entire discharge process rate. The peak-holding and constant current discharge circuit converts the input nuclear pulse signal into a single slope pulse signal.

The circuit simulation results shown in Fig. 1b indicate that there is a small non-linear region at the end of the discharge process, which is primarily determined by the Volt-Ampere (V-A) characteristics of the diode. When the forward voltage applied to the diode is less than the threshold voltage, the diode exhibits high impedance, and the forward current is nearly zero. When the applied voltage exceeds the threshold voltage slightly, the internal PN junction's built-in electric field of the diode is neutralized. Consequently, the diode exhibits low impedance and enters the forward conduction region. However, at this initial stage of conduction, the voltage and current are not yet fully proportional. As the external electric field continues to increase, the forward current of the diode increases rapidly, and the V-A (voltage-current) characteristics become approximately linear, indicating that the diode is now in full conduction. Once the diode is in the forward-biased conduction state, the forward voltage drop across it remains essentially constant.From the simulation diagram, it can be observed that during the signal discharge process, the fluctuation of the discharge current I_{dis} is less than 0.1μA, while the discharge current is 5.875μA. Testing has shown that the inherent non-linearity for signals with a peak-to-peak value of 0.4 V or greater is less than 0.05%, and the overall linearity is better than 0.1%. This signifies that the system has good linearity in converting amplitude values into time widths and responds well to small signals within a certain range, as illustrated in Fig. 1b.

The signal transformation circuit converts the single-slope pulse signal into a square wave signal that complies with the FPGA input levels,thereby facilitating the measurement of pulse width time. The transformation circuit employs a comparator to perform threshold comparison on the single-slope pulse signal outputted from the previous stage, converting it into a square wave signal.

The DC bias voltage V_b provides a DC offset of approximately 0.53V for the signal. The overall analog circuit noise is less than 10mV; therefore, the comparator voltage must be at least 0.54V to avoid the impact of noise on pulse width conversion. To test the relationship between the pulse width conversion circuit performance

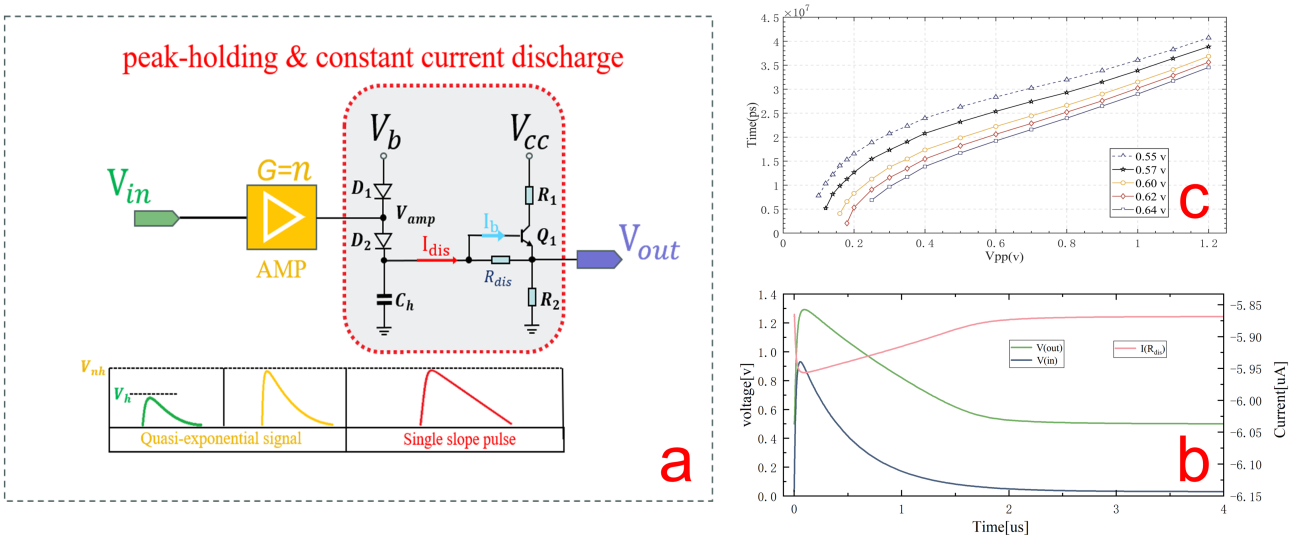

Fig. 1. **a** Schematic diagram of peak-holding and constant current discharge ,**b** The circuit simulation of the rapid charge and the constant discharge process ,**c** Test results of amplitude-time conversion at different comparator threshold levels.

and the setting of the comparator threshold, input amplitudes ranging from 0.1V to 0.2V were selected, with a test point every 20mV. from 0.2V to 0.4V, a test point was selected every 50mV, and from 0.4V to 1.2V, a test point was chosen every 100mV. At each test point, over 100000 sets of the sample data were collected. Additionally, different comparator threshold values were selected based on the actual signal discharge signal baseline for testing, specially 0.55V, 0.57V, 0.60V, 0.62V, and 0.64V. The final test results are shown in Fig. 1c.

From Fig. 1c, it can be observed that when the peak-to-peak value of the input signal is less than 0.4V, the relationship between the input signal amplitude and time does not exhibit a clear, linear one-to-one correspondence. The primary reason for this phenomenon can be attributed to the V-I (voltage-current) characteristics of the diode. According to the basic V-I characteristics of an ideal diode, when the forward voltage across the diode exceeds its forward voltage drop, the current through the diode undergoes an abrupt change. However, during actual testing, when the forward voltage is in the vicinity of the diode's critical conduction voltage, the diode exhibits a soft conduction phenomenon. This means that, when the forward voltage difference across the diode is slightly greater than the critical conduction voltage, the current does not undergo an abrupt change as per ideal diode characteristics; instead, it displays a nonlinear, smooth transition. Due to this soft conduction characteristic, when the peak-to-peak value of the input signal is relatively small, the relationship between V_{pp} (peak-to-peak voltage) and time is not entirely linear.

2.2 FPGA-TDC Design

The direct counting method utilizes a high-frequency clock to measure the width of the input signal. When the leading edge of the input signal arrives, the FPGA initiates counting, and halts it upon arrival of the trailing edge. By calculating the number of clock cycles elapsed between the start and end times, the time width of the input signal can be determined. Direct measurement of pulse width using clock counts offers a wide measurement range, but the period interval of the counting clock may introduce significant leading and trailing edge errors.

This paper utilizes the internal carry chain of the FPGA to construct a refined carry chain that precisely counts the leading and trailing edges of the pulse separately. A high-frequency clock is employed for coarse counting of the main pulse width, and the two counts are then summed to obtain the pulse width time. The carry chain is a fundamental structure within the FPGA. In the Xilinx Artix-7 series FPGA, the structure of the CARRY4 (Carry Chain Block 4) is depicted in Figure 2. Each CARRY4 consists of a carry multiplexer (MUXCY) and an XOR gate, which together generate carry signals. The CI (carry input) is connected to the carry output of the previous stage, while the CO (carry output) serves as the carry output of the CARRY4. The signal S controls the output of the MUXCY.

This design establishes a carry chain delay measurement by cascading CARRY4 units, capturing the internal tap signals of the CARRY4, and subsequently extracting fine count time through encoding and decoding processes.

By configuring the S[3:0] of CARRY4 to 1111, the four MUXCY input signals are programmed to select the cascaded carry input and the carry-out of the previous stage. This interconnection links the CO (Carry-Out)

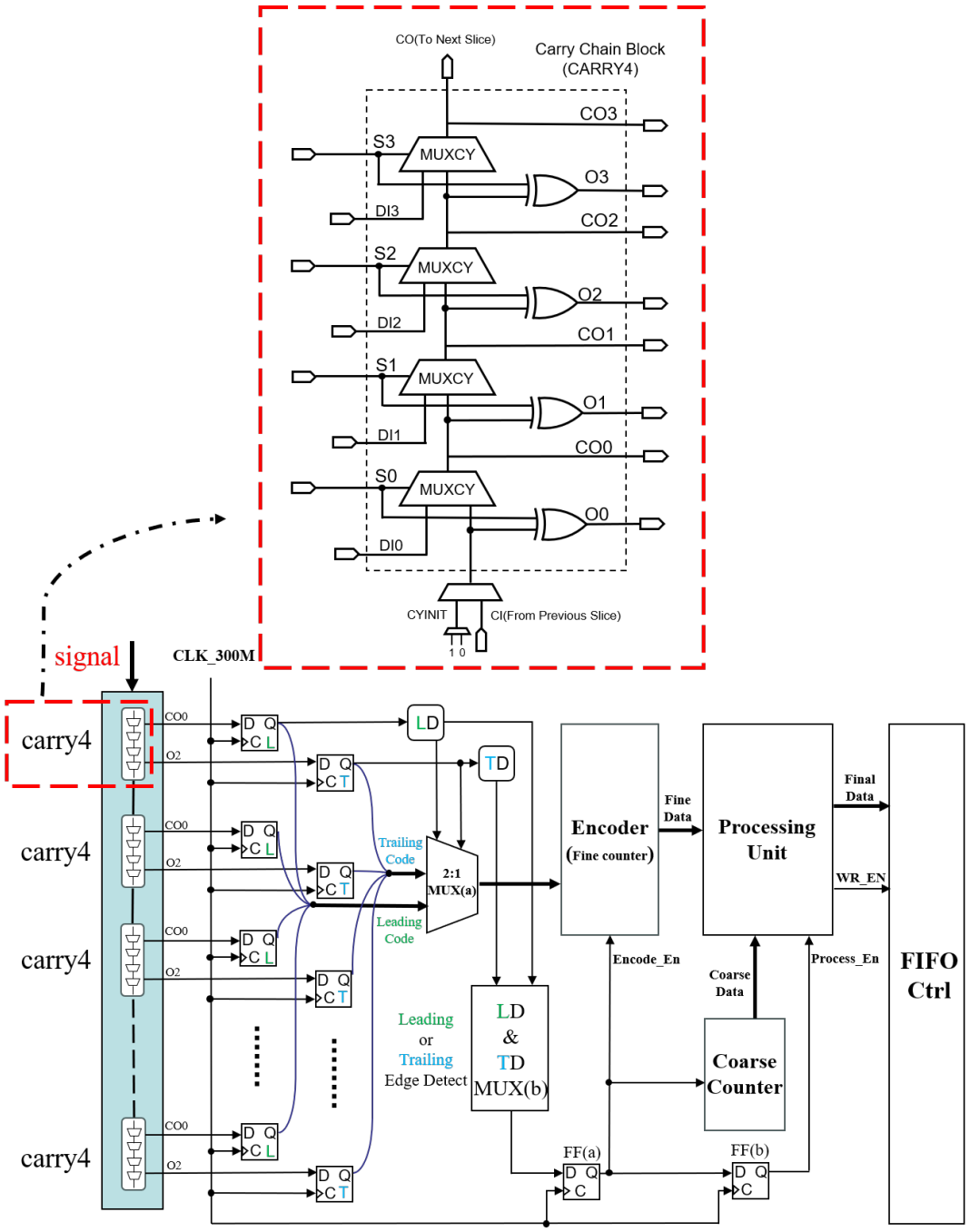

Fig. 2. Fast carry logic paths and related components in the A7 series FPGAs

with CI(Carry-In) within the CARRY4, froming a single CARRY4 delay module. Whitin this module the carry signal traverses from CI to CO is the minimum delay unit of the delay chain.

Within the CARRY4 carry chain, there are tap signals designated as O[3:0] and CO[3:0]. Upon the arrival of the leading edge of the measured signal, each MUXCY level triggers its corresponding CO output to transition from ”0” to ”1”. Conversely, When the trailing edge of the measured signal arrives, O becomes the XOR result of S and the carry signals CO and CI. Given that S is set to 1, O changes from ”0” to ”1”. Consequently, the CO and O tap signals’ sensitivity to the leading and trailing edges of the measured signal can be utilized to determine the precise moment of the square wave signal’s edge. This capability allows for the simultaneous measurement of both the leading and trailing edges of the signal using a single delay chain.

Fig. 2 depicts the specific design approach of the FPGA-TDC, which incorporates a fine counter for measuring the

temporal segments of both the front and back of the signal. In the initial delay unit, two delay flip-flops, TD and LD, are inserted to signify the valid leading edge or trailing edge. Following a delay of one clock cycle, the signal branches into two paths. One path directs to MUX(a) for selecting the encoding of the time signal's leading or trailing edge, while the other path passes through MUX(b) to choose the corresponding leading or trailing edge as a latch signal. Upon passing through flip-flop FF(a), the latch signal latches the result in the encoder and concurrently serves as the start and end signal for the coarse counting module.

The latch signal, after traversing another flip-flop FF(b), generates the enable signal "Process_En" for the Processing Unit module. Upon reaching the the Processing Unit, "Process_En" integrates the latched encoding result (fine count value) with the coarse count result to produce the final timing data, which is then written to the FIFO. Notably, no additional clocks are utilized during the encoding and data processing. Thus, the longest delay path of TD and LD spans from the edge indication signal to the FIFO write enable, consuming two system clocks. Consequently, the TDC designed in this paper boasts a maximum dead time of two clock cycles, significantly reducing the system dead time attributed to the TDC during measurement.In the A7 series FPGAs, each clock domain encompasses 50 slices, equivalent to 50 carry4 resources. The theoretical delay time from CI to CO in each carry4 is approximately 98ps[32], though actual measurements indicate a shorter duration. Prior to designing the delay chain, it is crucial to estimate the number of delay units and ensure it remains below 50 to prevent the delay chain from spanning across banks, which could result in uneven delays.

The Encoder module translates the time signal into a digital signal code, resulting in a thermometer code with a bit width equivalent to the carry chain, exemplified by "111111...00000". In the Processing Unit module, which includes a thermometer code decoding circuit, the time data is derived by counting the "1"s in the thermometer code. To enhance FPGA resource utilization and minimize system dead time during measurement, this paper adopts a binary search method for decoding the thermometer code. This method offers favorable time and space complexity, allowing for the swift and efficient identification of the transition point from "0" to "1" in the code[33].

Regarding the output signals from the detector, the majority fall within the system's dynamic range. However, a minority of signals exhibit intensities below the dynamic range's lower limit, particularly those with widths less than half of the sampling clock period. For these signals, the TDC measurement circuit may only capture one edge (leading or trailing) when attempting to detect both, resulting in inaccuracies. To address this challenge, an event assembly circuit, implemented using a finite state machine (included in the Processing Unit module shown in Fig. 2), is tasked with screening all signals to ensure data accuracy and completeness.

2.3 TDC Performance Test

2.3.1 TDC Code density and Non-linearity test

Due to the influence of manufacturing processes and layout routing, it is difficult for each delay unit in the FPGA's carry chain to have exactly the same delay time. Therefore, it is necessary to precisely calibrate the delay time of each delay unit in advance. To achieve this goal, the standard code density test method[34, 35] is commonly used to measure the delay characteristics of each delay unit.

A large number of pulses of randomly varying widths, uniformly distributed within [0, T], are used as test signals for the TDC (where T is the period of the standard system clock). If the delay time of each delay element were the same, when there are enough test samples, the number of signals falling on each delay element should be evenly distributed. However, since the delay time of each delay element varies, the uneven distribution of signals across the delay elements is determined by the additional delay time. By recording the total number of times each delay element is hit by events, we can determine the corresponding code density for each delay element.

Assuming there are enough test samples and ignoring the non-uniform distribution factors of the input signal, the delay time of each delay element is proportional to the number of pulses that fall into it. This means that the more times a random input signal falls into a particular delay unit, the longer its delay time and the greater its code density. Since the sum of the delay times of all delay units equals one reference clock cycle, by multiplying the proportion of the code density occupied by each delay unit with the sampling period T, one can determine the delay time of each delay unit in the delay chain.

To ascertain the precision and dependability of the measurement outcomes, it is imperative to establish the requisite number of test samples prior to conducting the tests. Suppose the range of values for the individual pulse signals is uniformly distributed across the interval[0,T_c], with P representing their probability density function, expressed as $P = \frac{T}{T_c}$. The likelihood of a pulse occurring within a specific delay element is directly proportional to the delay time T_d of that element, with the probability given by $P_d = \frac{T_d}{T_c}$. Given N events, the frequency of occurrence within delay element i is denoted by $n_i = NP_i = N\frac{T_i}{T_c}$.

By leveraging the relationship between the density of the delay element codes and the sampling interval, the delay time $\widehat{T_i}$ for the i-th delay element can be derived, as presented in Eq. (1).

$$\widehat{T_i} = \frac{n_i}{N} T_c \tag{1}$$

By tallying the number of events N_i that occur in each successive delay element, one can ascertain the delay times for all elements. Subsequently, summing the delay times of the initial i elements yields the cumulative delay time

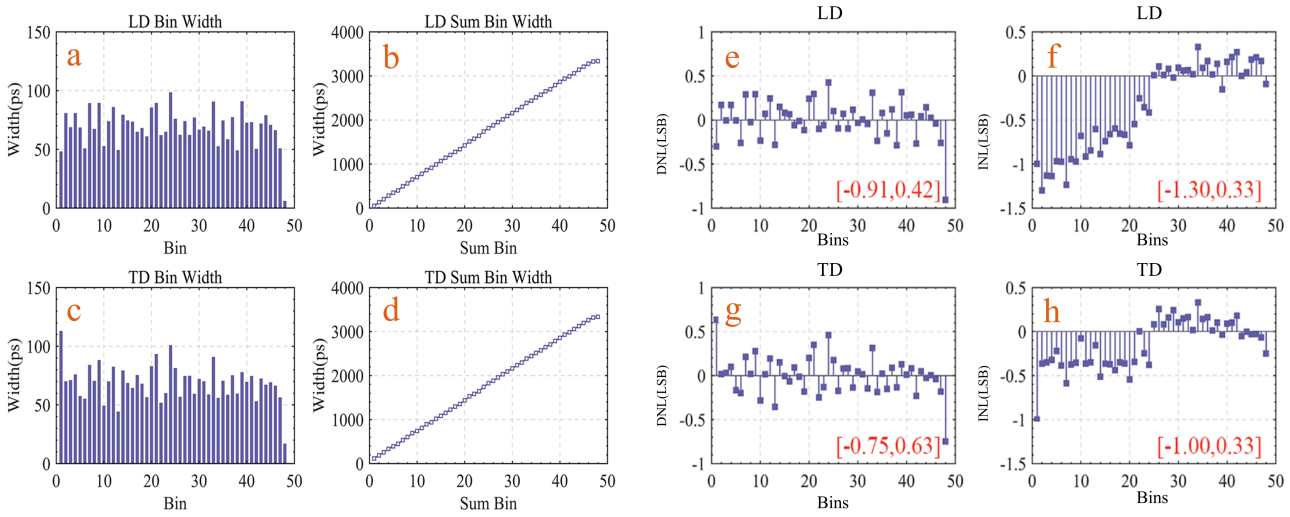

Fig. 3. **a** Leading edge code density of delay elements , **b** cumulative leading edge code density , **c** trailing edge code density , **d** cumulative trailing edge code density . **e** Leading edge differential nonlinearity of the delay chain , **f** leading edge integral nonlinearity , **g** trailing edge differential nonlinearity , **h** trailing edge integral nonlinearity .

t_i experienced by the pulse as it reaches each specific delay element, as detailed in Eq. (2).

$$t_i = \sum_{n=1}^{i} \widehat{T}_i = \sum_{n=1}^{i} \frac{n_n}{N} T_c \tag{2}$$

In practice, the edge of the test signal falls within the interior of the i delay element, so there will be an error regardless of whether t_i or t_{i-1} is chosen as the total delay time. Assuming the measured value is τ, then $t_{i-1}<\tau<t_i$, the variance σ^2 of τ is:

$$\sigma^2 = \frac{1}{t_i - t_{i-1}} \int_{i-1}^{i} (t-\tau)^2 dt = \frac{(t_i-\tau)^3 - (t_{i-1}-\tau)^3}{3(t_i - t_{i-1})} \tag{3}$$

In Eq. (3), the standard deviation δ^2 reaches its minimum value when $\tau = \frac{t_i - t_{i-1}}{2}$. At this point, the observed value is t, as shown in Eq. (4).

$$t = \sum_{n=1}^{i-1} \widetilde{T_n} + \frac{1}{2}\widehat{T_i} = \sum_{n=1}^{i-1} \frac{n_n}{N} T_c + \frac{1}{2}\frac{n_i}{N} T_c \tag{4}$$

Therefore, when a random signal falls within a delay element, the measured value should be taken at the midpoint of the delay element to minimize the standard deviation of the measurement value.

From (4), it is evident that an inadequate sample size results in excessive statistical errors, necessitating a specific requirement for sample size in code density testing. For a finite number N of test events, the event count n_i where the test pulse edge falls within a delay element follows a binomial distribution $D(N_i) = NP_i(1-P_i)$, with the expected value $\overline{n} = N \times P_i$ and the standard deviation $\sigma_{ni} = \sqrt{NP_i(1-P_i)}$.

Since all events are independent, the count values n_i are also independent. Therefore, using Eq. (2) and (4), we can derive Eq. (5).

$$\sigma_i = \sqrt{\sum_{n}^{i-1} \sigma^2 T_n + \frac{1}{2}\sigma^2 T_i} = \sqrt{\sum_{n}^{i-1} \sigma^2 n_n + \frac{1}{2}\sigma^2 n_i} \tag{5}$$

If the delay time of each delay element is equal, then the probability of a pulse falling on the i-th delay element is $P_i = \frac{1}{S}$, where S is the number of delay elements in a delay chain. When i=S, i is the last delay element in the delay chain, and at this point, σ_i reaches its maximum value σ_{max}.

$$\sigma_{max} < \frac{T_c}{N}\sqrt{S\sigma n_d^2} = \frac{T_c}{N}\sqrt{1 - \frac{1}{S}} \leq \frac{T_c}{\sqrt{N}} \tag{6}$$

Given that the external signal sampling clock designed in this study is 250 MHz, we have T_c=4000ps. To ensure that σ_{max} does not exceed 40ps, we set σ_{max}=40ps. Substituting this value into Eq. (6), we get N≥10000, which means the number of test events must not be less than 10000.

Hence, a signal generator is employed to generate 20000 random pulse width square waves. It is essential that the external sampling clock and the measurement sampling clock are not sourced from the same origin, and they should not be in an integer multiple relationship, as this would result in a fixed phase between them, which is inadequate for achieving complete randomness. The sampling clock is a 300 MHz clock generated by a PLL from an external crystal oscillator, with a period of 3.33 ns. According to the theoretical delay time of 98ps, 34 CARRY4 delay elements would be required. However,

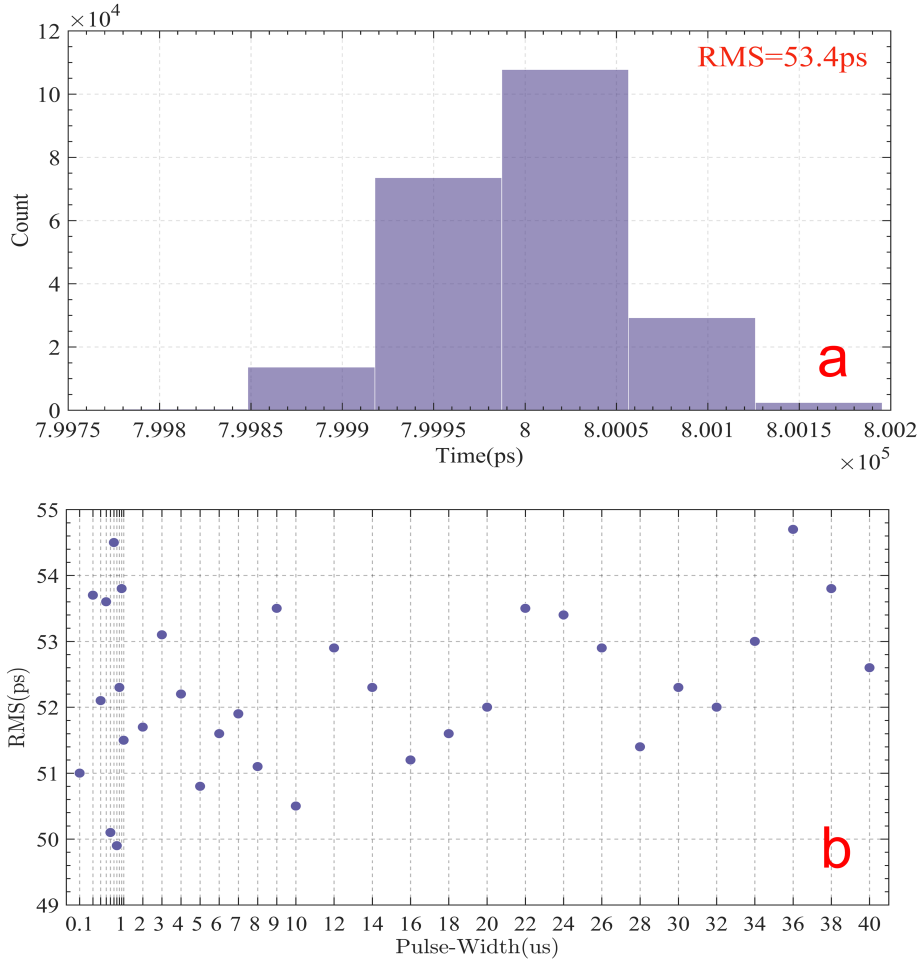

Fig. 4. **a** Signal width = 800ns, RMS test value , **b** 100ns $\leq$ signal width $\leq$ 40us, RMS test values at various test points.

after testing with random signals, it was found that at a clock frequency of 300 MHz, the actual delay time of each CARRY4 delay element is less than 98 ps. Therefore, for both the leading and trailing edges, there are effectively 48 delay elements, which is fewer than the maximum number of delay elements per bank mentioned earlier. Thus, using a 300MHz clock as the coarse counting clock can meet the design requirements, and the delay chain is theoretically expected to exhibit better linearity. The test results are shown in Fig. 3a-d.

If automatic layout and routing are performed using software, it is common for the delay chain to span different Banks, leading to uneven delays. The test results in Fig. 3a-d show the code density test results after manual layout and routing, where the distribution of each delay element is more uniform. The delay differences between each delay element are mainly attributed to the time differences in the sampling clock reaching various registers, as well as the inherent non-uniformity of the semiconductor manufacturing process.

The nonlinear performance of a TDC is primarily assessed using two metrics: Differential Nonlinearity (DNL) and Integral Nonlinearity (INL). These parameters reflect the uniformity of the TDC's bin widths. Fig. 3e-h illustrates the DNL and INL of delay units in a manually routed delay chain within a digital circuit. The formulas for calculating DNL and INL are as follows:

$$DNL_i = \frac{LSB_i - LSB}{LSB}, \tag{7}$$

$$INL_i = \frac{\sum_{i=0}^{n} LSB - iLSB}{LSB} \tag{8}$$

In this context, LSB_i refers to the delay time corresponding to the i-th delay element. When analyzing this section, LSB_i represents the number of measured pulses for the corresponding delay element, and the time resolution is the average number of pulses.

The differential nonlinearity for the leading edge is optimized to the range [-0.91, 0.42], and the integral nonlinearity is [-1.30, 0.33]. For the trailing edge, the differential nonlinearity is [-0.75, 0.63], and the integral nonlinearity is further optimized to the range [-1.0, 0.33].In an ideal scenario, the delay time of each delay unit that

constitutes a TDC should be identical, which implies that the width of all bins should be exactly the same. The smaller the bin width, the higher the resolution of the TDC. The average resolution of a TDC can be represented by Eq. (9), which takes into account the uniformity of all delay units and the impact of bin width on resolution.

$$LSB = \frac{T_c}{N}, \tag{9}$$

In the TDC delay chain, N represents the number of effective delay units within the time T_c. For a given TDC delay chain with 48 effective delay units, and a sampling clock of 300MHz for each delay unit, which is T_c=3333.3ps. The average resolution of the delay chain is LSB=69.4ps.

2.3.2 RMS accuracy analysis

By conducting multiple measurements within a fixed time period and analyzing the dispersion of the resulting data, the root mean square (RMS) accuracy of TDC measurement data can be assessed. RMS accuracy is an important metric for evaluating the precision of TDC measurement results in characterizing pulse width signals. RMS accuracy reveals the degree of deviation of the measured values from the ideal values. The calculation of RMS follows Eq. (10):

$$RMS = \frac{1}{\sqrt{N-1}}\sqrt{\sum_{i=1}^{N}(X_i - \frac{\sum_{i=1}^{N} X_i}{N})^2} \tag{10}$$

Where N denotes the number of measurements, and X_i represents the data from the i-th measurement. The more data tested for a pulse of the same time width, the more accurate the calculated RMS value becomes. Fig. 4a shows the RMS test results for a square wave signal with a pulse width of 800 ns, with an RMS value of 53.4 ps.

To comprehensively evaluate the performance of the TDC designed in this study over a wide range of times, we adopted a strategy of selecting test points in stages: within the 0 to 1us range, a test point was set every 100 ns; within the 1 to 10us range, a test point was set every 1 us; within the 10 to 40 us range, a test point was set every 2 μs. This distribution of test points ensures an accurate assessment of the TDC's performance across different time scales. At each test point, we collected more than 100,000 sets of sample data to ensure the statistical reliability of the data. Through the analysis of this data, we obtained the distribution of time measurement accuracy results as shown in Fig. 4b.

Based on these measurement data, we calculated that the average accuracy of the TDC designed in this study in time measurement is 52.3 ps. This result not only demonstrates the high performance of the TDC in the time range from nanoseconds to microseconds but also verifies its application potential in the field of high-precision time measurement.

Using the same precision evaluation method as mentioned above, we added three more measurement channels identical to it in the system and tested the other three channels in the same way. Under the condition that all test conditions remain unchanged, the measurement results of time precision for each TDC channel are shown together. The measurement results indicate that the average precision of the four TDC measurement channels is approximately 50ps in the range of 100 ns to 40 us.

2.4 Gamma-ray spectrometry measurement and analysis.

In this study, we selected the CH132-07 type NaI(Tl) scintillation detector produced by Beijing Hamamatsu Photonics as the signal input source. This detector is equipped with a crystal of size Φ25mm$\times$25mm, and its energy resolution for the characteristic peak of ^{137}Cs is better than 9% (nominal energy resolution). During the experiment, we used the "TDC scheme" and the "ADC scheme" for comparison. In the experiment, we utilized ^{131}I and ^{137}Cs radioactive sources for energy calibration. The energy spectra obtained by these two schemes are shown in Fig. 5.

In the TDC scheme, the comparator threshold was set to 0.64V. After energy calibration, it can be observed that the energy spectrum results of the TDC scheme and the ADC scheme coincide at the high, medium, and low energy characteristic peaks. The two characteristic peaks corresponding to the energies of 365keV and 662keV from ^{131}I and ^{137}Cs in the energy spectrum measurement results of the two schemes are clearly distinguished, and the peak positions of the characteristic peaks coincide. Under the same test conditions, the energy resolution of the ADC scheme for the characteristic peak of ^{137}Cs is 8.3%, while the resolution of the TDC scheme designed in this paper for the characteristic peak of ^{137}Cs is 8.5%.

3 Summary

This paper proposes a high-precision Time-to-Digital Converter (TDC) for use in a digital multichannel analyzer. By using this method, the digital multichannel analyzer quantifies and collects statistics on the discharge time of nuclear pulse signals, ultimately obtaining the gamma energy spectrum. Experimental results show that on a Xilinx A7 series FPGA, the TDC resolution can reach 69.4ps, the dead time is two system clocks, the differential nonlinearity range of the leading edge measurement of the delay chain is [-0.91, 0.42], and the integral nonlinearity range is [-1.30, 0.33]; the differential nonlinearity range of the trailing edge measurement is [-0.75, 0.63], and the integral nonlinearity range is [-1.0, 0.33]. An analysis of the key parameters in the circuit's impact on the results reveals that, for signals

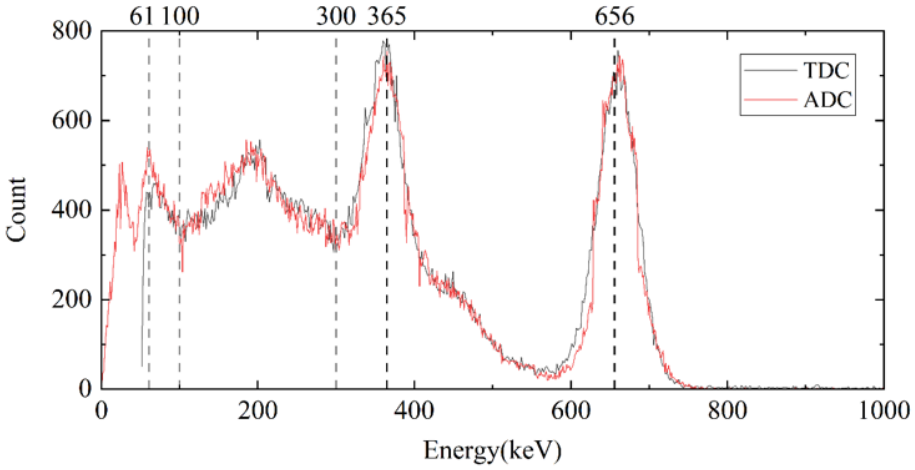

Fig. 5. Comparison of spectral measurement between ADC scheme and TDC scheme.

with voltages higher than 0.4V, the nonlinearity of the conversion results of the autonomous linear discharge circuit is less than 0.05%. Tests were conducted using a NaI(Tl) detector with a size of ϕ25mm$\times$25mm, alongside a linear discharge circuit and a high-precision TDC for the measurement of the 662keV full-energy peak of the ^{137}Cs source, with an energy resolution of 8.5%. Under the same measurement conditions, the energy resolution measured using the ADC scheme was 8.3%. The analysis of the experimental results demonstrates the feasibility of the proposed method in the context of digital multichannel analyzers. Through innovating the front-end analog circuit, a compact and structurally simple autonomous linear discharge analog scheme is proposed, where the autonomous linear discharge structure, combined with the use of high-precision FPGA-TDC, provides a new solution for the acquisition and measurement of multi-channel system.

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